MOLECULAR LOGIC GATES

TECHNICAL FIELD

The present invention is related to molecular electronics and, in particular, to resistor-based nanoscale logic circuits that provide easily distinguished logic output signals in response to the logical states of an arbitrary number of logical input signal lines.

BACKGROUND OF THE INVENTION

During the past fifty years, tremendous progress has been made in electronic technologies. Large vacuum-tube-based electronic systems were replaced with smaller, more reliable transistor-based electronics, in turn replaced with integrated-circuit technologies with ever increasing component densities and switching speeds. Currently, efforts are being made to push the standard photolithographic semiconductor-fabrication process to produce ever decreasing components sizes. One approach to decreasing component sizes is to decrease the wavelength of the light used to expose photoresist in photomasking steps. Retooling current semiconductor-fabrication facilities to employ shorter wavelength, soft x-rays is projected to involve staggering capital expenditures. Moreover, various physical limits of component sizes may be soon approached. For these reasons, designers and manufacturers of electronics systems, and, in particular, manufacturers and designers of computer processors and memories, are currently seeking non-photolithographic technologies for producing denser electronic circuitry.

A new approach to circuit fabrication involves molecular electronics. Nanoscale molecular wires ("nanowires") can now be fabricated into programmable nanoscale crossbars and other structures, with molecular junctions at nanowire interconnections, comprising as few as 40 molecules, providing resistor-like, diode-like, and transistor-like nanoscale components. Efforts are currently underway to fabricate high-density logic circuits, memory elements, programmable gate arrays, and processors using these new nanoscale technologies. However, at nanoscale dimensions, precise fabrication of molecular-junction diode and transistors presents

many challenges. Designers and manufacturers of nanoscale electronic circuits, including logic circuits and memories, have therefore recognized the need for basic, reliable molecular logic gates despite current difficulties in reliably fabricating nanoscale diode and transistor components.

SUMMARY OF THE INVENTION

In one embodiment of the present invention, an alternating current ("AC") source is superimposed on a direct-current ("DC"), largely resistor-based nanoscale logic circuit in order to provide distinguishable, AC current or voltage logical output signals despite potentially narrow DC-voltage or DC-current ranges produced by the resistor-based nanoscale logic circuit. AC-enhanced AND, OR, NAND, and NOR nanoscale logic gates are provided as four specific embodiments of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-D functionally illustrate the four, basic logic gates AND, OR, NAND and NOR.

Figure 2 illustrates a desirable, wide-signal-range property of a generalized logic gate.

Figure 3 illustrates a rectifying diode.

Figures 4A-D illustrate an example AND logic gate with four input signals lines that would be desirable to fashion at the molecular level.

Figures 5A-D illustrate, in a fashion similar to Figures 4A-D, implementation of a diode-based OR gate.

Figures 6A-D illustrate operation of a resistor-based OR logic gate.

Figure 7 illustrates an enhancement to the OR-logic-gate implementation shown in Figures 6A-D that provides a distinguishable output-signal-line voltage state.

Figure 8 illustrates the threshold, second-input-signal-line voltages needed for the enhanced implementation of the logic gate shown in Figure 7 in order to produce OR and AND logic gates.

Figure 9A illustrates an AC-enhanced, nanoscale NOR logic gate that represents one embodiment of the present invention.

Figure 9B illustrates the general principle of operation of the AC-enhanced, nanoscale NOR logic gate shown in Figure 9A, and of other AC-enhanced, nanoscale logic gates shown in subsequent figures.

Figures 10A-C illustrate operation of the AC-enhanced, nanoscale logic gate shown in Figure 9.

Figure 11 shows an AC-enhanced, nanoscale AND logic gate implementation that represents one embodiment of the present invention.

Figures 12A-C illustrate operation of the AC-enhanced, nanoscale AND logic gate shown in Figure 11.

Figure 13 shows an AC-enhanced, nanoscale logical OR gate that represents on embodiment of the present invention.

Figure 14 illustrates an AC-enhanced, nanoscale NAND logic gate that represents one embodiment of the present invention.

Figure 15 shows an AC-enhanced, mixed-logic circuit that represents an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

One embodiment of the present invention provides nanoscale logic gates that produce logical output signals with relatively wide voltage or current ranges that lead to readily electronically distinguishable ON and OFF logical output signals. Four specific embodiments, provided below, include AND, OR, NAND, and NOR nanoscale logic gates.

Figures 1A-D functionally illustrate the four, basic logic gates AND, OR, NAND and NOR. Figure 1A shows an AND logic gate. The AND logic gate is symbolically represented as a semi-rectangularly shaped closed figure with one rounded side 102 to which a number of signal lines 103-106 are input and from which a single output signal line 108 emerges. Each input signal line 103-106 may be in a high-voltage or high-current state, normally considered a logical ON state, or a low-voltage or low-current state, normally considered a logical OFF state. These states

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are alternatively represented as Boolean "1" and "0," respectively. An opposite convention may also be used.

As with all logic gates, the voltage or current state of the output signal line 108 depends on the logic states of the input signal lines. The AND logical gate 102 shown in Figure 1A has four input signal lines, but AND logical gates may have between two and an arbitrary number n input signal lines. The logical state of the output signal line 108 for each possible combined state of the input signal lines is provided in the chart 110, to the right of the symbolic representation of the AND gate in Figure 1A. The output signal line is ON when all n input lines are also ON. Figures 1B-1D illustrate the OR, NAND and NOR logical gates using the same illustration conventions as used for Figure 1A. The output signal line of an OR logical gate 112 is OFF only when all n input lines are OFF. The output signal line 114 of a NAND logical gate is OFF only when all n input signal lines are ON. The output signal line 116 of a NOR logical gate 116 is ON only when all n input signal lines are OFF.

Figure 2 illustrates a desirable, wide-signal-range property of a generalized logic gate. In Figure 2, a general logic gate 202 receives four input signal lines 203-206 and produces a single output signal line 207. The input signal lines 203-206 are each in either a high-voltage or high-current ON state, or in a low-voltage or low-current OFF state, as represented by the bar-graph-like chart 208 to the left of the generalized logic gate. It is desirable that the difference Δ 210 between the 0 and 1 states is relatively large, so that 0 and 1 logic states can be unambiguously electronically distinguished. Similarly, the output signal line 207 may also be either in an ON or OFF state, with well-separated voltage or current differences 212 between the 0 and 1 states. As with a manufactured article, components and subcomponents of logic gates cannot be manufactured with precise dimensions, material composition, and physical characteristics, but instead exhibit ranges of physical characteristics within certain design and manufacturing tolerances. Therefore, the 0 and 1 voltage or current states of input signals to a logic gate exhibit a more or less continuous range of current or voltage distributed about the ideal 0 current or voltage and the ideal 1 current or voltages. As the difference Δ between the

voltage or current representing logical 0 and 1 decreases, the potential ambiguity of the combined state of the input signals may increase. If logic gates, in turn, produce output signals with narrowed voltage or current ranges, the ambiguity may be amplified through propagation within a logic circuit comprising many tens, hundreds, thousands, or millions of logic gates. Therefore, a large Δ is desirable, both in input signal lines and in output signal lines. More particularly, the output-signal-line Δ of a logic gate should be at least as large as that of any input signal line.

Figure 3 illustrates a rectifying diode. A rectifying diode is represented by a filled triangle and a vertical line symbol 302. Diodes are commonly used as rectifying components that pass DC current in only one direction. When a diode is forward biased, as shown in Figure 3A, with a higher voltage on the anode side of the diode 304 then on the cathode side of the diode 306, there is a forward voltage drop V_f across the diode, and the diode passes a forward current i_f in the direction of the forward voltage bias. Conversely, when the diode is reversed biased, as shown in Figure 3D, with a higher voltage on the cathode 308 side of the diode than on the anode 310 side of the diode, there is a potential drop V_r across the diode essentially equal to the applied reverse biasing voltage. When reversed biased below a breakdown threshold, the diode passes only a tiny 312 reverse current i_r. The diode thus serves as a one-way gate, passing substantial current only in one direction. When forward biased, as shown in Figure 3A, the diode is in a low impedance state, as a result of a narrowed depletion region within the pn junction forming diode, thus allowing the diode to pass a relatively small AC signal superimposed on the forward biasing DC current in either the forward or reverse directions. However, when the diode is reversed biases, as shown in Figure 3B, the depletion region within the pn junction of a diode is broadened, resulting in a high-impedance state that blocks propagation of a relatively small AC signal superimposed on the reverse biasing DC current in either direction.

Figures 4A-D illustrate an example AND logic gate with four input signals lines that would be desirable to fashion at the molecular level. In Figure 4A, a voltage source 402, which provides the ON logic-state voltage V_{CC}, is coupled to a first resistive element 404 with resistance R_1, in turn coupled to the output signal line

406 and the four input signal lines 408-411, and to ground through a second resistive element 412 with resistance R_2. Each of the four input lines 408-411 are gated with diodes 414-417. When all four input signals are ON, at the relatively high voltage V_{CC}, as shown in Figure 4B, none of the four diodes 414-417 are forward biased, and

5   therefore the output signal line 406 has the voltage level $\dfrac{R_1}{R_1 + R_2} V_{CC}$ which

approaches V_{CC} when the resistance R_2 of resistive element 412 is significantly less than the resistance R_1 of resistive element 404. However, as shown in Figure 4C, when any one input signal line is in a low-voltage state, then the diode gating that signal line becomes forward biased and essentially shorts the output signal line to the

10   low-voltage state. In the example shown in Figure 4C, the first input signal line 408 is shown to be grounded 410, thereby forward biasing diode 414, with a voltage drop across diode 414 of V_f. Therefore, the output signal line 406 is at a relative potential V_f. Generally, the voltage drop across a forward-bias diode is quite small in comparison with a driving voltage V_{CC}, and consequentially the potential V_f

15   represents a low-voltage, OFF state. Figure 4D shows both the first and second input lines 408 and 409 in OFF states, with the relative potential of the output signal line 406 equal to $V_f - \Delta$, where Δ is a small positive additional voltage drop resulting from the second forward-biased diode.

        The AND logical gate implementation illustrated in Figures 4A-D is

20   an example of a logic gate with easily distinguished output logical states, as discussed above with reference to Figure 2. Figures 5A-D illustrate, in a fashion similar to Figures 4A-D, implementation of a diode-based OR gate. The OR gate includes four input signals lines 502-505, each gated with a diode 506-509, and each interconnected with the output signal line 510 and to ground 512 through a resistive element 514. As

25   shown in Figure 5B, when all four input signal lines are in the OFF logical state, or, in other words, interconnected with ground 516-519, then the output signal line 510 has a voltage potential of 0. However, as shown in Figure 5C, when a single input signal line, for example input signal line 502, has the logical state ON, or, in other words, has the relatively high voltage potential V_{CC}, then the diode gating the signal

30   line 506 is forward biased, and passes, to the output signal line 510, the high voltage

state V_{CC} with a small voltage drop due to the diode 506. In the case that all four input signal lines are ON, as shown in Figure 5D, then the output signal line 510 has the voltage potential $V_{CC} - V_f + \Delta$, where Δ is a relatively small positive adjustment. Thus, again, the diode-based logic circuit provides output voltage states that are easily distinguished, since the voltage range is essentially 0 to V_{CC}.

Both the example AND and OR logic gates described above with references to Figures 4A-5D have only four input signal lines, each of which are gated with diode elements. As discussed above, these relatively simple implementations provide the wide voltage ranges needed for easily distinguishing ON and OFF states on the output signal line produced by the logic gates. However, there are several problems that prevent current use of these simple diode-based implementations at nanoscale dimensions. First, while diode-like molecular junctions can currently be fabricated, these diode-like molecular junctions may not have sufficient functional yield and sufficient reliability to provide for feasible commercialization. A second, contributing factor is that, in general, logic gates may need to support a large number of input signal lines n, where n is much greater than four. Due to the difficultly in producing nanoscale diode elements, a nanowire-crossbar-type logic gate with n input signals can currently be manufactured only with very low yields and reliability, due to the multiplicative decrease in yield due to the individual defect and failure probabilities associated with single diode-like molecular junctions. However, it is currently feasible to manufacture reliable resistive molecular junctions at the molecular level. Thus, resistor-based logic gates are potentially commercially feasible. However, the logical state of output signal lines emerging from resistor-based logic gates may not be easily distinguished.

Figures 6A-D illustrate operation of a resistor-based OR logic gate. This logic gate is similar to the OR logic gate described above, with reference to Figures 5A-D, with the exception that each of the four input signal lines 602-605 include resistive elements 606-609 rather than the diode elements included in the diode-based implementation shown in Figures 5A-D. As shown in Figure 6A, when all four input signal lines are OFF, the output signal line 610 is also OFF. As shown in Figure 6B, when a single input signal line, for example, signal line 602, is ON, at a

voltage of V_{CC}, then the output signal line 610 is at the relative voltage $\frac{1}{5}V_{CC}$. As shown in Figure 6C, when two input signal lines 602 and 604 are ON, the output signal line is at the relative voltage $\frac{2}{5}V_{CC}$. Finally, as shown in Figure 6D, when all four input signal lines are ON, the output signal line is at the relative voltage $\frac{4}{5}V_{CC}$.

5   Thus, in the resistor-based implementation, the voltage ranges between 0 and $\frac{4}{5}V_{CC}$, and is relatively evenly distributed through that range depending on a number of input signal lines that are ON. In the case shown in Figures 6A-D, the output-signal-line voltage 0 represents logical OFF, and the output-signal-line voltage $\frac{1}{5}V_{CC}$, and all higher output-signal-line voltages, represent the logical state ON. The resistor-based

10   implementation has a voltage range of $\frac{1}{5}$ V_{CC}, and has therefore decreased the voltage difference between the ON and OFF states by nearly $\frac{4}{5}V_{CC}$.

Figure 7 illustrates an enhancement to the OR-logic-gate implementation shown in Figures 6A-D that provides a distinguishable output-signal-line voltage state. As shown in Figure 7, the four input signal lines are connected to

15   one input 702 of a comparator 704, and the other input of the comparator 706 is interconnected to a variable-resistance subcircuit including a resistor 708 and a voltage source 710. The variable-resistance subcircuit allows the second input signal line 712 connected to the second input 706 of the comparator 704 to be placed precisely at a threshold voltage. The comparator 704 outputs ON when the voltage at

20   the first input 702 is equal to or greater than the voltage at the second input 706, and otherwise outputs OFF. Thus, setting input signal line 712 to a constant voltage of $\frac{1}{10}V_{CC}$ allows the enhanced circuit to function as an OR logic gate, and setting the input signal line to the second input 706 of the comparator 704 to the constant voltage of $\frac{7}{10}$ V_{CC} allows the enhanced logic gate shown in Figure 7 to function as an AND

logic gate. Note that the threshold voltage input to the second input 706 of the comparator 704 is set to a voltage value intermediate between the two voltage states output from the resistor-based logic gate that correspond to ON and OFF voltage states.

Figure 8 illustrates the threshold, second-input-signal-line voltages needed for the enhanced implementation of the logic gate shown in Figure 7 in order to produce OR and AND logic gates. In Figure 8, the output-signal-line voltage state corresponding to the number of signal lines that are in the ON state is shown for the case of n signal lines input to the logic gate. Therefore, the voltage separation between n-1 and n input signal lines in the ON state is $\frac{1}{n+1}V_s$, where V_s is the source voltage. Therefore, to produce an OR logic gate, the threshold voltage is set midway between voltage levels 0 and $\frac{1}{n+1}V_s$, or $\frac{1}{2n+2}V_s$ 802. In order to produce an AND logic gate, the threshold voltage is placed intermediate between the voltage state for n-1 input signal lines in the ON state and n signal lines in the ON state, or $\frac{2n-1}{2n+2}V_s$ 804. As is evident from Figure 8, the ability to distinguish the ON and OFF states of the resistor-based logic gate decreases with an increasing number of input signal lines. Because the voltages of the input signal lines cannot be precise, but fall in a distribution around 0 and V_s, there is a limit, even in the enhanced logic gate shown in Figure 7, to the number of input signal lines that can be accommodated by the logic gate without producing a voltage separation between output logical states that is too narrow.

Figure 9A illustrates an AC-enhanced, nanoscale NOR logic gate that represents one embodiment of the present invention. In the AC-enhanced, nanoscale NOR logic gate, four input signal lines 902-905 are interconnected, through resistor-like elements 906-909, to an alternating current input source 910, the output signal line 912, and a diode-like element 914 slightly forward biased by a biasing DC voltage source 916. Note that the terms "diode-like" and "resistor-like" indicate that the elements are nanoscale analogs to microscale and macroscale diodes and resistors, but not necessarily having all characteristics similar to the larger scale analogs. In

certain embodiments, the diode-like element may be a larger-than-nanoscale element interconnected with numerous nanoscale logic gates. The AC-enhanced logic gate produces AC current or voltage logical states on the output signal lines, superimposed over a DC current or voltage signal, depending on whether voltage or current signals

5   are employed in the logic circuit in which the AC-enhanced, nanoscale NOR logic gate is included. In general, the logical states of the DC input signal lines 902-905 determine whether or not the diode 914 is fully forward biased. The AC current or voltage logical output signal superimposed on a DC output signal may be converted to either a pure AC logical signal or, more commonly, to a DC logical signal via an

10   AC-to-DC signal converter.

Figure 9B illustrates the general principle of operation of the AC-enhanced, nanoscale NOR logic gate shown in Figure 9A, and of other AC-enhanced, nanoscale logic gates shown in subsequent figures. An AC-enhanced logic gate, at a simplified, conceptual level, comprises an AC current source 920, a first signal line

15   921 connected to a resistor 922 with resistance $\dfrac{R}{n}$, where n is the number of input

signal lines, in parallel with a second signal line 923 connecting a diode 924 whose incremental conductance depends on the DC bias, and an output signal line 926. The diode is generally slightly forward biased by a DC biasing source 928. The diode may have low impedance Z_{low} and high impedance Z_{high} states, with the impedance

20   changing from Z_{low} to Z_{high} as the voltage rises above a threshold voltage V_{thresh}. Table 1, below, shows the impedance states of the diode produced by various levels and polarities of biasing:

bias voltage	Z
reverse (bias < 0)	Z_{high}
0	Z_{high}
slightly forward ($0 < $ bias $ < V_{thresh}$)	Z_{high}
fully forward (bias $> V_{thresh}$)	Z_{low}

25   Table 1

The first and second signal lines carry DC current and voltage, with the resulting polarity and magnitude of the voltage difference between the anode and cathode sides of the diode determining the impedance of the diode. The AC current on the output signal line I_{out} is:

$$I_{out} = I_{source} - I_{\frac{R}{n}} - I_D$$

$$= I_{source} - \frac{nV_{source}}{R} - V_{source}g_D$$

where g_D is the incremental conductance of the diode.

In general, the impedance of a resistor connecting an input signal line to the AC-enhanced logic gate is relatively large. When the diode is in a high-impedance state, both of the latter two negative terms are relatively small, and the output current I_{out} is close to I_{source}, provided that n is not too large. When the diode is in a low impedance state, the output current I_{out} is small, and approaches 0. Therefore, the DC voltage states of the first and second signal lines determine whether or not the diode is fully forward biased, and therefore whether the AC output signal is close to I_{source}, or ON, or close to 0, or OFF.

Figures 10A-D illustrate operation of the AC-enhanced, nanoscale logic gate shown in Figure 9. In Figure 10A, all four input signal lines 902-905 are in the OFF logical state, essentially at a DC voltage of 0, and therefore the diode 914 is not forward biased, and presents high impedance to the AC source 910. As a result, output signal line carries a relatively high AC signal, or, in other words, is in the ON logical state. In Figure 10B, the first input signal line 902 is ON, with an input DC voltage of V_{cc}. The diode 914 is therefore forward biased, and presents low impedance to the AC source 910. The AC signal on the output signal line 912 is, as a result, relatively low, or, in another words, the output signal line is in the OFF logical state. Similarly, as shown in Figure 10C, when all input signal lines are ON, the output signal line remains in the OFF logical state.

Figure 11 shows an AC-enhanced, nanoscale AND logic gate implementation that represents one embodiment of the present invention. In Figure

11, the AC voltage source 1102 produces a voltage or current signal that is either shunted to the output signal line 1104 or essentially shorted to ground through the diode 1106, depending on whether or not the diode is forward biaed to the low impedance state. The diode 1106 is slightly forward biased by the biasing DC source 1108 and fully forward biased by the additional, much larger, DC source 1110. Figures 12A-C illustrate operation of the AC-enhanced, nanoscale AND logic gate shown in Figure 11. In Figure 12A, all four input signal lines 1208-1211 are OFF. Therefore, the diode 1106 is fully forward biased, presenting low impedance to the AC signal source 1102. The AC source is essentially shorted to ground, leaving the output signal line 1104 in an OFF AC logical state. As shown in Figure 12B, when the first input signal line 1208 is ON, and the remaining input signal lines 1209-1211 are OFF, the voltage at node 1212 is substantially less than V_{CC}, since input signal line 1208 is essentially shorted to ground through input signal lines 1209-1211. As shown in Figure 12C, only when all four input signal lines 1208-1211 are ON is the DC voltage at node 1212 close to V_{CC}, balancing the opposite polarity DC source 1110 so that the diode 1106 is only slightly forward biased. The diode therefore presents high impedance to the AC source 1102, resulting in a high AC output voltage (logical ON) to the output signal line 1104.

Figure 13 shows an AC-enhanced, nanoscale logical OR gate that represents on embodiment of the present invention. In Figure 13, the diode 1302 is only fully forward biased by the fully forward biasing bias source 1303 when all four input signals 1304-1307 are OFF. Otherwise, when any one or more of the input signal lines 1304-1307 are ON, with DC voltage V_{cc}, the voltage at node 1312 is larger, and in opposite polarity, to the bias voltage, and the diode is consequently not forward biased, and therefore presents high impedance to the AC source 1308. Therefore, the output signal line 1310 is ON when one or more of the input signal lines is ON, and is OFF when all four of the input signal lines are OFF.

Figure 14 illustrates an AC-enhanced, nanoscale NAND logic gate that represents one embodiment of the present invention. In Figure 14, the diode 1402 would be fully forward biased by the biasing DC voltage source 1403, but is reverse biased by the larger voltage V_{cc} source 1401. When any one or more of the input

signal lines 1404-1407 are OFF, the voltage at node 1408 is insufficient to forward bias the diode 1402. Therefore, only when all four input signal lines are ON is the output signal line 1410 OFF, while, when any one or more of the input signal lines 1404-1407 is OFF, the output signal line 1410 is ON.

Although the present invention has been described in terms of a particular embodiment, it is not intended that the invention be limited to this embodiment. Modifications within the spirit of the invention will be apparent to those skilled in the art. For example, an almost limitless number of different logic circuits incorporate one of the logical-gate embodiments described above. For example, Figure 15 shows an AC-enhanced mixed-logic circuit that produces an ON output signal when inputs X0 and X1 are OFF and input Z0 is ON. The AC-enhanced molecular logic-gate implementations incorporate only a single diode element, despite the number of input signal lines. A single-diode-nanoscale circuit can be manufactured with greater reliability, and correspondingly higher yield, then a multiple-diode-nanoscale circuit, as discussed above. Moreover, the single diode element may be a sub-micron diode manufactured using a different technology than the molecular-wire-implementation of the nanoscale logic gate. Additional configurations of logic circuits that produce AC-enhanced logic circuits are possible. In alternative embodiments, a transistor may be used to switch AC current to the output signal line, rather than a diode. Many other types of components and component configurations are possible that produce nanoscale logic gates with well separated AC logical signal states. Embodiments of the present invention may be employed in nanoscale and mixed nanoscale/microscale logic circuits, processors, programmable gate arrays, memories, and other types of electronic devices and circuits.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. The foregoing descriptions of specific embodiments of the present invention are presented for purpose of illustration and description. They are not intended to be exhaustive or to limit the invention to the

precise forms disclosed. Obviously many modifications and variations are possible in view of the above teachings. The embodiments are shown and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents: